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**BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES**

Application Number: 10/074,064

Filing Date: February 12, 2002

Appellant(s): ASARO ET AL.

Christopher J. Reckamp
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 11/21/08 appealing from the Office action mailed 11/21/07.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

5857083	Venkat	1-1999
5859987	Gillespie	1-1999
6094699	Surugucchi et al	7-2000
6,675,292	Prabhu et al	1-2004

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.
2. Claims 1, 4-9, 19, 22-23, 25-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gillespie et al PN 5,859,987 in view of Surugucchi et al PN 6,094,699 and Venkat PN 5,857,083.

In regards to claims 1, 8, 19: Gillespie et al teaches a data bridge system, comprising: an interface (interface to primary PCI bus 9 or alternatively interface to local memory bus 11) for transferring data; a plurality of application-specific integrated circuits (ASICs) (21 and 23); a data bridge operatively coupled to each of the interface and the plurality of ASICs (7). Gillespie et al also teaches the bridge accessing a ROM storing configuration (31 Column 1 lines 59-65). Gillespie et al does not expressly teach the data bridge read only memory storing at least initial values and mask values for each ASIC of the plurality of ASICS. The examiner notes Gillespie et al does teach the bridge having a plurality of Base address registers in accordance with the AGP and PCI specifications, which would inherently need to be configured. Surugucchi et al

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teaches a bridge (210 or alternatively 210 and 212 taken together) including a mask register storing mask values for masking Base address registers in accordance with the attached peripherals. It would have been obvious to store the configuration mask values in the data bridge ROM of Gillespie et al because this would have consolidated configuration. Venkat teaches storing the initial base addresses in the configuration space of the devices. It would have been obvious to store the initial values in the configuration space of the combination of Gillespie et al in view of Surugucchi et al because this would have consolidated necessary configuration data.

In regards to claims 4, 22: Gillespie et al teaches the bridge having Base address registers. (part of the PCI specification incorporated in Gillespie)

In regards to claims 5-6, 23, 26: Gillespie et al teaches multiple base address registers in accordance with the PCI specification incorporated by reference in Gillespie et al. The PCI specification notes the number of Base address registers in a bus bridge is 6.

In regards to claims 7, 25: Gillespie et al teaches multiple base address registers in accordance with the PCI specification which teaches the base address registers having prefetchable and non-prefetchable and I/O space and non I/O space determinations. PCI specification page 196.

In regards to claim 9: Gillespie et al teaches a configuration EEPROM. Which is an electrically erasable programmable ROM.

In regards to claim 27: Gillespie et al does not teach the EEPROM being removable.

MPEP 2144.04 V C states to make separable is not a patentable distinction.

3. Claims 2-3, 20-21, 24, 33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gillespie et al PN 5,859,987 in view of Surugucchi et al PN 6,094,699 and Venkat PN 5,857,083 as applied to claim 1 above, and further in view of Applicants admitted prior art.

In regards to claims 2, 20, 24, 33: Gillespie et al does not teach the ASICs being graphics processors. Applicants admitted prior art teaches graphics processors (1020) attaches to a bus. It would have been obvious to include graphics processors because this would have allowed for the efficient control of graphics/video.

In regards to claims 3, 21: Gillespie et al in view of Surugucchi et al and Venkat teach the bridge attached to a AGP bus described above. Gillespie et al in view of Surugucchi et al and Venkat do not teach a north bridge. Applicants admitted prior art teaches a north bridge attaches an AGP bus. It would have been obvious to a person of ordinary skill in the art at the time of the invention to use the bridge of Gillespie et al in view of Surugucchi et al and Venkat in the system of Applicants admitted prior art because this would have separated the graphics from the PCI system thus freeing the PCI system.

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4. Claim 28 is rejected under 35 U.S.C. 103(a) as being unpatentable over Prabhu et al PN 6,675,292 in view of what is well known in the art.

In regards to claim 28: Prabhu et al teaches forming (configuring) a configurable register (Control register that is configured in Column 5 lines 41-56) that includes register configuration logic (the register is configurable as read/write or read only, whatever allows/does the configuration is the configuration logic) and at least one register flop to contain an initial value (inherent when the register is configured as read only if it had no initial value then the only possible value would be 0000. The examiner notes 0000 can also be an initial value) and at least one mask flop (indication of read only or read/write. the binary item that indicates the register is read only) that generates a mask bit (read only indication) for the configuration logic and wherein the register configuration logic configures the at least one register flop to be read only or read writable based upon the at least one mask value (if it is set as read only then the value in the register is read only). Prabhu et al does not expressly teach the initial value and whether it is to be read only or read writable being stored in a memory only the configuring the register as read only. Official notice is taken that configuration memory is well known. It would have been obvious to a person of ordinary skill in the art at the time of the invention to store the configuration info in a memory because this would have given it some place to come from.

5. Claims 10-11, 13, 15-17, 34-35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gillespie et al PN 5,859,987 in view of Surugucchi et al PN 6,094,699 and Venkat PN 5,857,083 as applied to claim 1 above, and further in view of Prabhu et al PN 6,675,292.

In regards to claims 10-11, 34-35: Gillespie et al in view of Surugucchi et al and Venkat teaches the configurable bridge as described above including the configuration registers. Gillespie however does not expressly state the configuration registers are themselves configurable. Prabhu teaches configurable registers as described above. It would have been obvious to a person of ordinary skill in the art to make the registers themselves configurable because this would have provided for greater configuration control.

In regards to claims 13, 16: Gillespie et al teaches multiple base address registers in accordance with the PCI specification incorporated by reference in Gillespie et al. The PCI specification notes the number of Base address registers in a bus bridge is 6.

In regards to claim 15: Gillespie et al teaches multiple base address registers in accordance with the PCI specification which teaches the base address registers having prefetchable and non-prefetchable and I/O space and non I/O space determinations. PCI specification page 196.

In regards to claim 17: Gillespie et al teaches a configuration EEPROM. Which is an electrically erasable programmable ROM.

6. Claims 14, 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gillespie et al PN 5,859,987 in view of Surugucchi et al PN 6,094,699, Venkat PN 5,857,083 and Prabhu et al PN 6,675,292 as applied to claim 10 above, and further in view of Applicants admitted prior art.

In regards to claims 14 and 18: Gillespie et al does not teach the ASICs being graphics processors. Applicants admitted prior art teaches graphics processors (1020) attaches to a bus. It

would have been obvious to include graphics processors because this would have allowed for the efficient control of graphics/video.

In regards to claim 12: Gillespie et al in view of Surugucchi et al and Venkat teach the bridge attached to a AGP bus described above. Gillespie et al in view of Surugucchi et al and Venkat do not teach a north bridge. Applicants admitted prior art teaches a north bridge attaches an AGP bus. It would have been obvious to a person of ordinary skill in the art at the time of the invention to use the bridge of Gillespie et al in view of Surugucchi et al and Venkat in the system of Applicants admitted prior art because this would have separated the graphics from the PCI system thus freeing the PCI system.

(10) Response to Argument

In regards to applicants arguments regarding claims 1,4-9,19,22-23, and 25-27 that “what Gillespie would actually inherently need is that base address registers be populated with data values”: The registers of Gillespie are “config regs” meaning configuration registers. When a configuration register is populated with data values this is called configuring. Any time a configuration register is populated with data values the register is “configured”. The applicants appear to be trying to redefine the word configured to not include writing data to a configuration register. Populating a configuration register with values is by definition configuring. The word configure is defined as: To design, arrange, set up, or shape with a view to specific applications or uses. American Heritage dictionary 3rd edition. When a configuration register is populated

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with data it is set up with a view to specific applications or uses. The breadth of the claim language is so as to encompass simply writing configuration data into a register.

In regards to applicants argument that in Gillespie "There is no need for mask values that configure registers to be read and or writable": The examiner notes this argument is in regards to claims 1, 4-9, 19, 22-23, and 25-27. However none of these claims include the limitation of the mask value configuring the register to be read and/or writable. This limitation only appears in the allowed claims, in claims 28 and 34-35 which are addressed below.

In regards to applicants argument that "the Surugucchi reference appears to have been misapprehended. Surugucchi is directed to a different system from that taught by Gillespie or Applicants' claimed invention": Gillespie is directed to configuring the configuration registers by populating them with stored configuration information from EEPROM 31 in a PCI to PCI bridge. The examiner notes Gillespie expressly states that the bus is PCI thus these configuration registers are required to include the AGP/PCI Base Address Registers BAR. Surugucchi is directed to configuring the Base address registers in a Local bus to PCI bridge including in the configuration information is the BAR mask values. So that the registers store mask values. They are both directed to configuring configuration registers in PCI bridges.

In regards to applicants argument that the "mask registers" of Surugucchi merely stores values not mask values and "The mask values in Surugucchi have nothing to do with creating a register to be readable or writable": None of these claims include the limitation of the mask value configuring the register to be read and/or writable. Only that they include mask values. Which Surugucchi expressly teach setting the mask values for the PCI BAR registers. Gillespie teaches configuring a PCI-PCI bridge configuration registers by writing in the data from an

EEPROM. Gillespie does not teach what can be in this configuration data. Surugucchi teaches configuring a PCI bridge with mask values from a mask register. The examiner notes applicant is repeatedly arguing that the mask value of Surugucchi has nothing to do with making the register read or writable. The only claims that has this limitation are the allowed claims and claim 28 which was rejected over different art. Applicants are arguing features not claimed.

In regards to applicants argument that Surugucchi does not teach the values come from a ROM: The examiner agrees Gillespie teaches this feature.

In regards to applicants argument that Surugucchi teaches no more than what Gillespie teaches and “that Gillespie admittedly does not teach the claimed subject matter”: The examiner states that Gillespie does not expressly teach the mask values being included in the configuration information. While the examiner recognizes that Gillespie in all likelihood does inherently includes the initial mask values in the configuration information. Gillespie however did not expressly state that mask values were used. The examiner therefor cited Surugucchi since it expressly taught this feature.

In regards to applicants arguments regarding the rejection of claims 28 and 34-35: The examiner notes that this claim has removed the limitations of the register being in a bridge and now reads to be on any register. The breadth of claim 28 only requires that there is a configurable register with initial values stored therein, that it has a bit that indicates if it is read only or read/write and that there is a memory from which this configuration information comes. Any register that is configurable as either read only or read write would read on this claim language. Prabhu et al expressly teaches that many registers may be configured as read only. Thus Prabhu et al teaches a configurable register (“many registers may be configured”) that

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includes register configuration logic (“may be configured” this would require logic to do this) and at least one register flop (Registers are a series of register flops with each bit being called a flop) to contain an initial value (Even 0000 is a value. What the initial value is, is not taught but a register cannot be a register without an initial value) and at least one mask bit (the bit that indicates that the register is “configured as read only”) for the configuration logic (“may be configured”) and wherein the register configuration logic configures the at least one register flop to be read and or writable based on at the at least one mask value (“may be configured as read only” thus may also be configured as read only or read/write). The only thing Prabhu et al fails to teach is where the configuration information comes from.

In regards to applicants argument “that Prabhu is directed to an exception handling operation for SIMD floating point instruction using a floating point status register to report exceptions – not to data bridge systems and not to the claimed subject matter”: Applicants are arguing features that are not claimed. Claim 28 is for “A circuit”. This could be any circuit there is no requirement in the claim that the circuit be in a data bridge system.

In regards to applicants argument “that the cited paragraph of Prabhu actually refers to a preconfigured register block”: Preconfigured is configured it does not matter when the configuration of the register is done only that it is done. It doesn't matter if the register is configured by logic before it is installed in the system or later, it is still configured and the claim language does not state when it is configured only that the configuration is done. Prabhu teaches that configuration is done. Further to set a write protect bit (read or read/write) is well within the ordinary capabilities of one skilled in the art.

In regards to applicants argument “that there are no mask flops that generate a mask bit for any configuration logic in Prabhu as alleged”: Prabhu expressly states that the register “may be configured as read only” The bit that indicates the register is read only is the claimed mask bit since the scope of the claim language is broad enough to encompass even a simple write protect bit or a bit as in Prabhu that something that indicates the register is read only which in a digital system can only be one or more bits.

In regards to applicants argument that the “claim requires that the configuration logic configures the register flop to be read and/or writable based on at least one mask value stored in memory”: Prabhu teaches the register “may be configured as read only” When it is being configured, the circuit that performs this function would have no choice but to be called configuration logic (this circuit is inherent for a register to be able to be configured).

In regards to applicants argument regarding the word “forming”: The examiner has reviewed applicants specification to determine the meaning of the word forming in light of the applicants specification and the claim language and has concluded that the claimed forming is simply propagating the register flops with values. See applicants specification paragraph [0024-0025] and abstract and figure 3. This is how the examiner previously interpreted this word if it is meant to have a different definition than is supported by the specification the examiner was unable to determine it. The examiner has no choice but to accept populating a register with a value as the claimed forming a register.

Thus, Appellant's arguments are not considered persuasive towards patentability of the claims presented for consideration.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

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